CLAIMS

1. An integrated circuit for scan driving being used in sequentially selecting and driving scanning lines in a display, which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration, and which has a pixel arranged at each cross point; in this integrated circuit for scan driving, comprising:

a chip, having plural output pads arranged as a column in a first direction, plural drive circuits for driving said signal lines to the active state through said output pads, respectively, and plural selection circuits for individually selecting said driver circuits in a line-sequential scanning cycle in an order corresponding to the order of said signal lines;

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region,

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second region adjacent to said first region in said first direction;

said first region, in an order corresponding to the order of said odd-numbered signal lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, and, at the same time, said output pads, driver circuits and selection circuits corresponding to the scanning lines are arranged in the same row in the second direction nearly orthogonal to said first direction;

and, in said second region, in an order corresponding to the order of said even-numbered signal lines, said even-numbered output pads, driver circuits and selection circuits are arranged as columns in said first direction, and, at the same time, said output pads, driver circuits and selection circuits corresponding to the signal lines being arranged in the same row in said second direction.

2. The integrated circuit for scan driving as in Claim 1 comprising:

said odd-numbered selection circuits are made of individual flip-flops that overall form the first shift register; the first shift data provided by the frame period is transferred sequentially to the latter-stage flip-flops in synchronization with the first transfer clock signal at a frequency half that of the line-sequential scanning cycle; by means of the output signals of the flip-flops with said first shift data latched in them, the corresponding driver circuits are selected;

said even-numbered selection circuits are made of individual flip-flops that overall form the second shift register; the second shift data provided by frame period is transferred sequentially to the latter-stage flip-flops in synchronization with the second transfer clock signal at a frequency half that of the line-sequential scanning cycle and in a phase opposite to that of said first transfer clock signal; and, by means of the output signals of the flip-flops with said second shift data latched in them, the corresponding driver circuits are selected.

3. The integrated circuit for scan driving as in Claim 2 wherein said first and second shift registers allow bidirectional transfer of, respectively, said first and second shift data.

4. The integrated circuit for scan driving as in Claim 1 wherein said integrator circuit includes:

a transfer clock generator that divides the fundamental clock signal that defines the cycle of line-sequential scanning in half,

and a shift data generator that generates said first and second shift data in two consecutive cycles of said fundamental clock signal corresponding to the start pulse that indicates the timing of the start of a frame.

5. The integrated circuit for scan driving as in Claim 1 wherein said first direction corresponds to the longitudinal direction of said chip, and said output pads are arranged as a column along one edge extending in the longitudinal direction of said chip.

6. The integrated circuit for scan driving described in Claim 5 wherein the input pads for input of the desired power source voltage or signal are arranged as a column along the other edge in the longitudinal direction of said chip.

7. The integrated circuit for scan driving as in Claim 3 wherein said chip is assembled by means of TCP.

8. A type of integrated circuit for scan driving for sequentially supplying scan drive signal to the scanning electrodes of a display device; comprising:

a first shift register, which has plural register circuits connected in series, and which sequentially transfers the first shift data corresponding to the first clock signal,

a first drive section, which has plural driver circuits corresponding to the plural register circuits of said first shift register, respectively, and which has said plural driver circuits output drive signals corresponding to said first shift data output from the plural register circuits of said first shift register, respectively,

a second shift register, which has plural register circuits connected in series, and which sequentially transfers the second shift data shifted in phase by half a period of said second clock signal with respect to said first shift data corresponding to the second clock signal with its phase deviated by 180(from said first clock signal,

and a second drive section, which has plural driver circuits corresponding to the plural register circuits of said second shift register, respectively, and which has said plural driver circuits output drive signals corresponding to said second shift data output from the plural register circuits of said second shift register, respectively;

said drive signals are output alternately from the various driver circuits of said first drive section and the various driver circuits of said second drive section, corresponding to said first or second shift data.

9. The integrated circuit for scan driving as in Claim 8 wherein the register circuits of said first shift register and the driver circuits of said first drive section are arranged in order of activation along the first direction; and the register circuits of said second shift register and the driver circuits of said second drive section are arranged in order of activation along said first direction.

10. The integrated circuit for scan driving as in Claim 9 wherein said first and second shift registers are bidirectional shift registers that allow transfer of shift data bidirectionally; said first shift data is supplied to the register circuit in the initial stage or the register circuit in the final stage of said first shift register, and said second shift data is supplied to the register circuit of the initial stage or the register circuit of the final stage of said second shift register.

11. The integrated circuit for scan driving as in Claim 8 wherein said integrated circuit has a signal generator, to which the reference clock signal having a frequency double that of said first and second clock signals as well as a start pulse are input, and which generates said first and second clock signals and said first and second shift data on the base of said reference clock signal and said start pulse.

12. The integrated circuit for scan driving as in Claim 8 wherein said first and second shift registers and said first and second drive sections are formed on a rectangular semiconductor chip, and said first direction is the longitudinal direction of said semiconductor chip.

13. The integrated circuit for scan driving described in Claim 12 wherein the odd-numbered drive signals are sequentially output from the various driver circuits of said first drive section, and the even-numbered drive signals are sequentially output from the driver circuits of said second drive section.